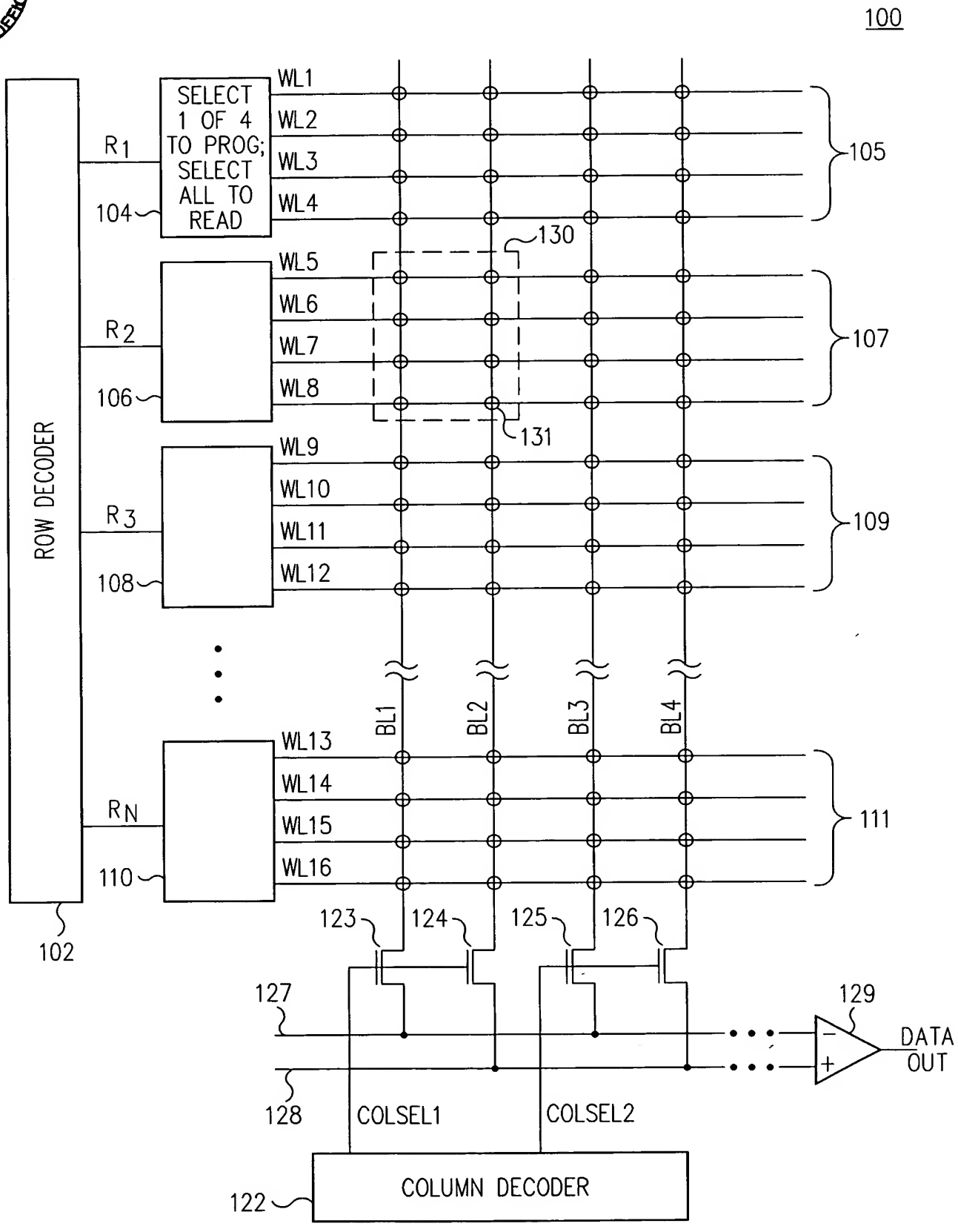
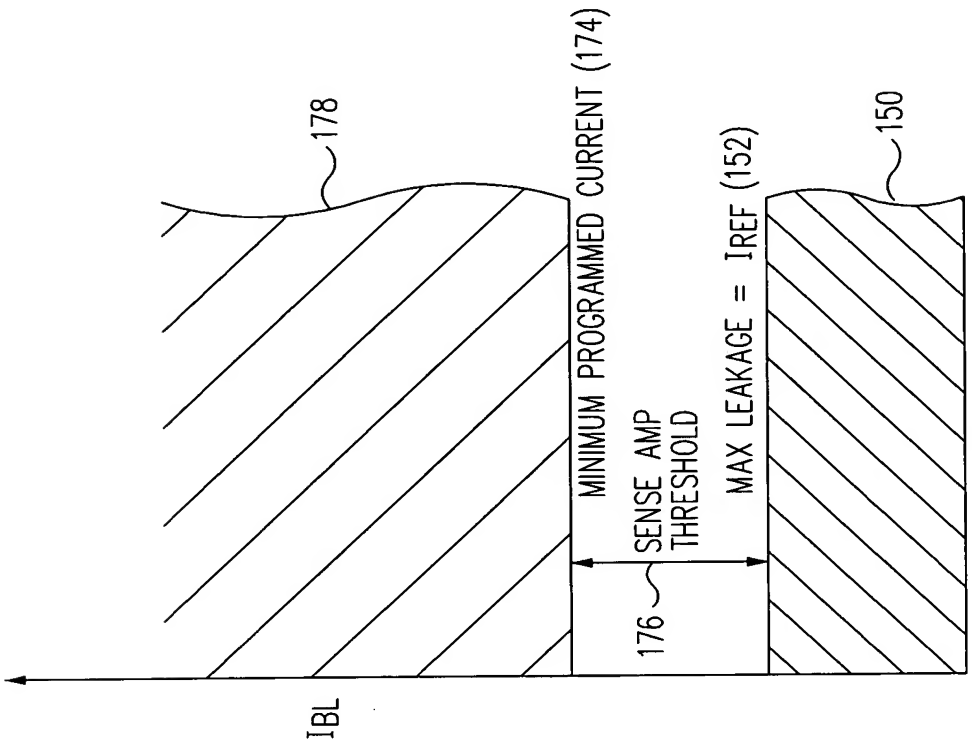
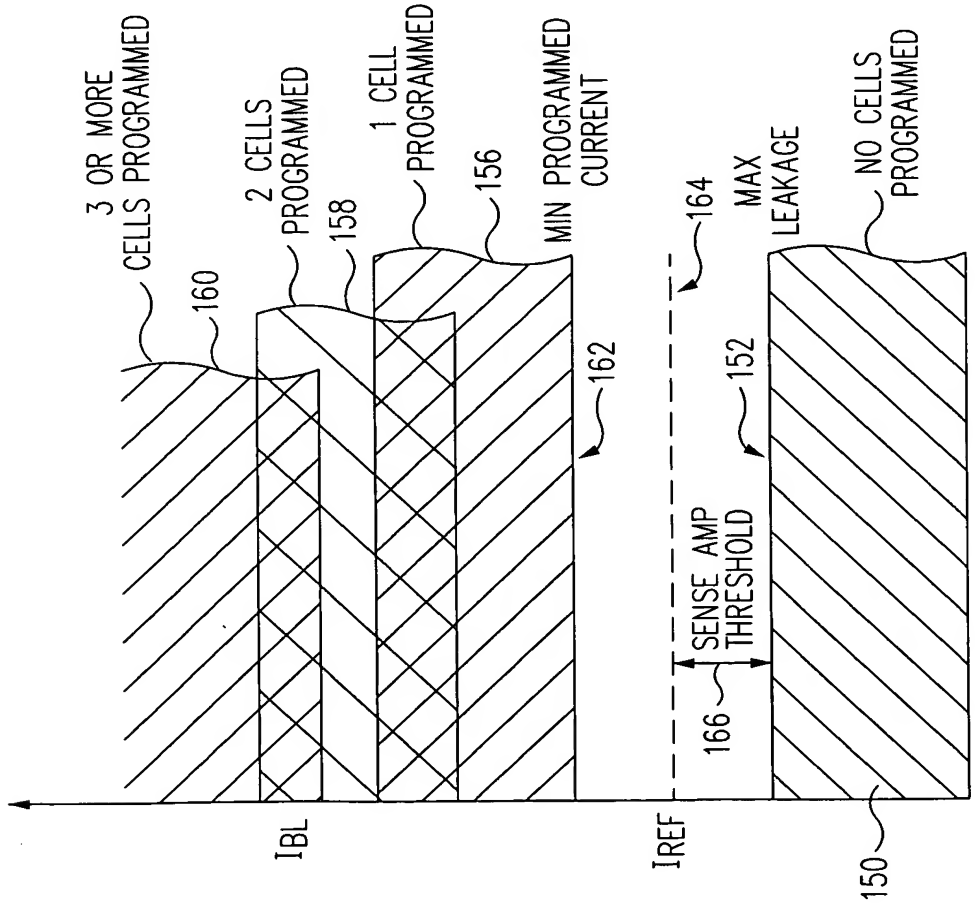


FIG. 1



TWIN CELL

FIG. 3



BINARY DECISION WITH REFERENCE

FIG. 2

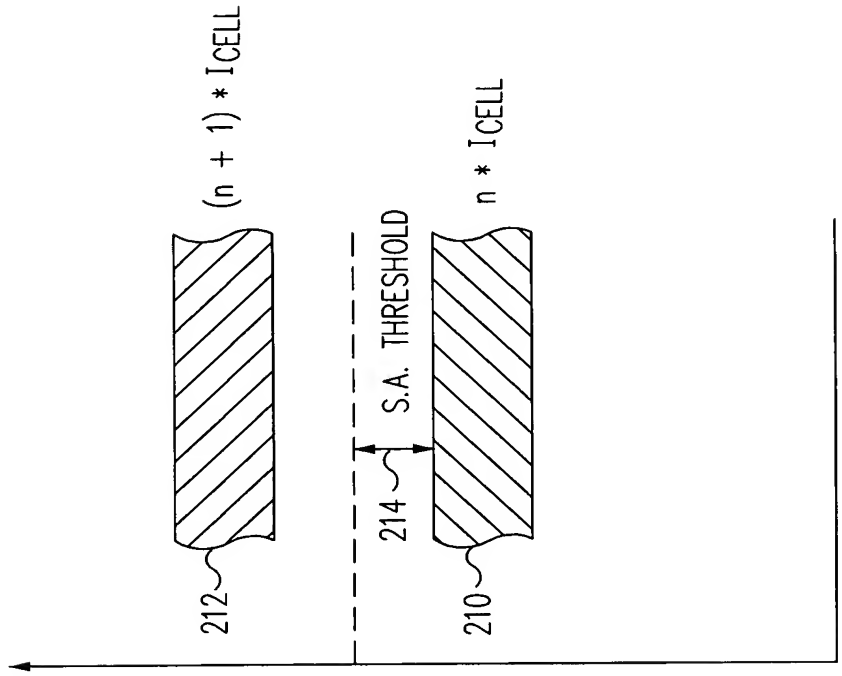

(n + 1) * ICELL
n * ICELL
S.A. THRESHOLD
214
212
210
SPREAD < IREF

FIG. 5

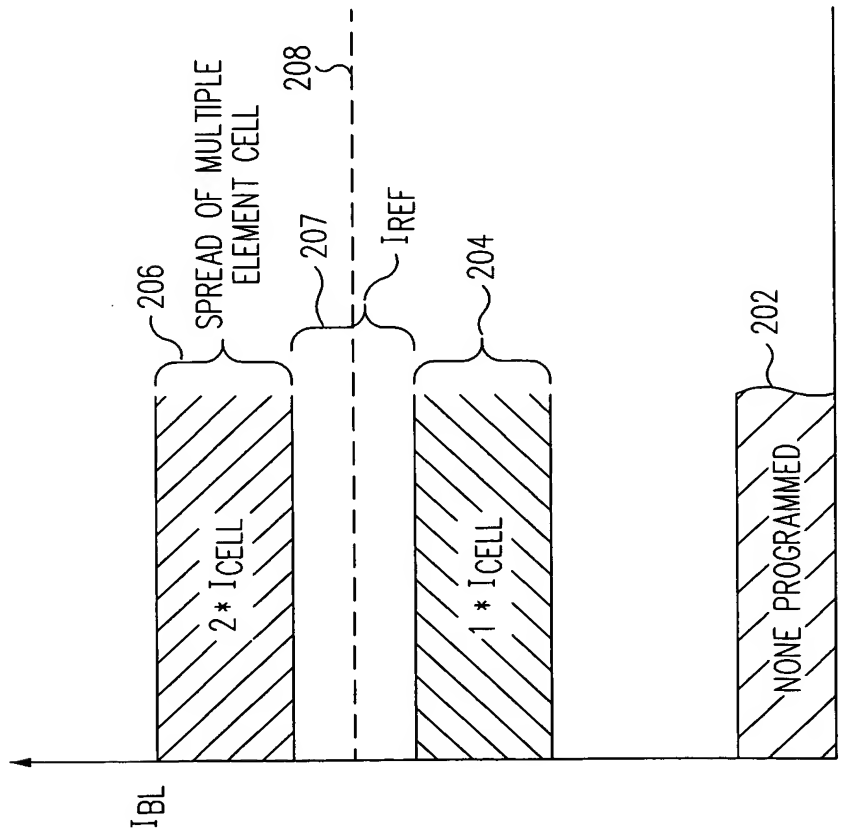

IBL
206
SPREAD OF MULTIPLE
ELEMENT CELL
208
207
IREF
204
202
2 * ICELL
1 * ICELL
NONE PROGRAMMED
SPREAD > IREF

FIG. 4

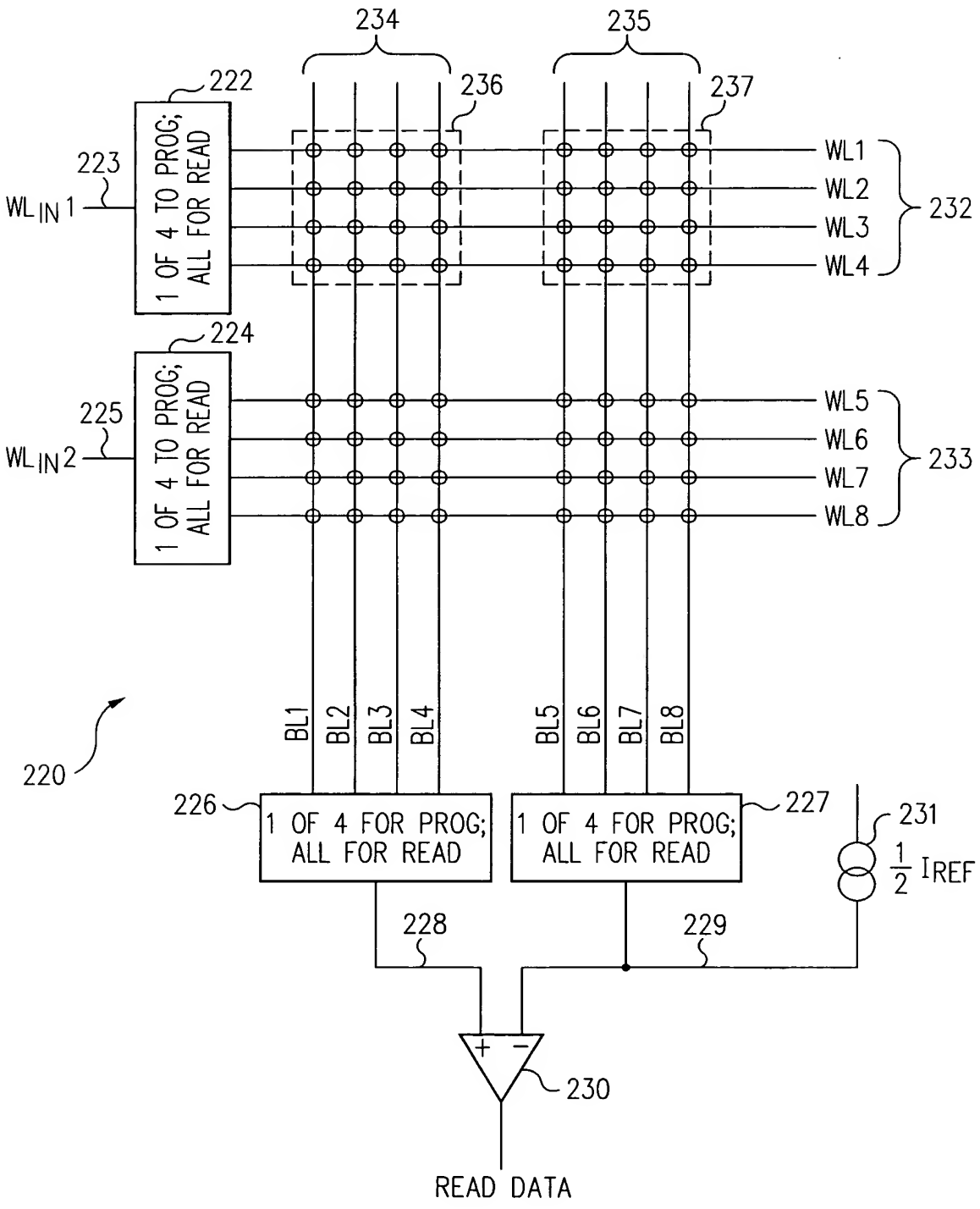

234
235
222
236
237
223
WL IN 1
1 OF 4 TO PROG; ALL FOR READ
WL1
WL2
WL3
WL4
232
224
225
WL IN 2
1 OF 4 TO PROG; ALL FOR READ
WL5
WL6
WL7
WL8
233
220
BL1
BL2
BL3
BL4
BL5
BL6
BL7
BL8
226
1 OF 4 FOR PROG; ALL FOR READ
227
1 OF 4 FOR PROG; ALL FOR READ
231
1/2 IREF
228
229
+
−
230
READ DATA

FIG. 6

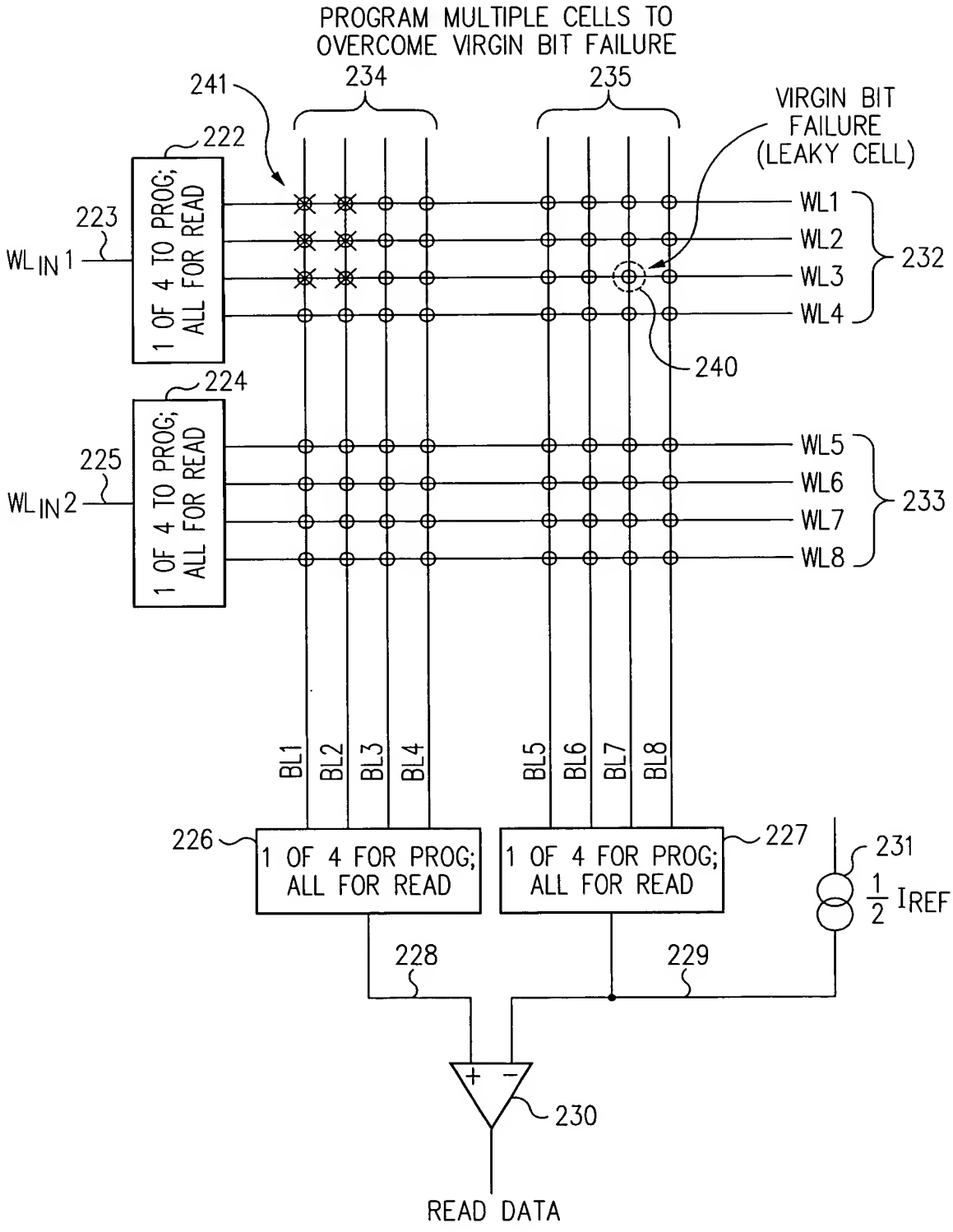

PROGRAM MULTIPLE CELLS TO
OVERCOME VIRGIN BIT FAILURE
241
234
235
VIRGIN BIT
FAILURE
(LEAKY CELL)
222
223
WL IN 1
1 OF 4 TO PROG;
ALL FOR READ
WL1
WL2
WL3
WL4
232
240
224
225
WL IN 2
1 OF 4 TO PROG;
ALL FOR READ
WL5
WL6
WL7
WL8
233
BL1
BL2
BL3
BL4
BL5
BL6
BL7
BL8
226
1 OF 4 FOR PROG;
ALL FOR READ
227
1 OF 4 FOR PROG;
ALL FOR READ
231
1/2 IREF
228
229
230
READ DATA

FIG. 7

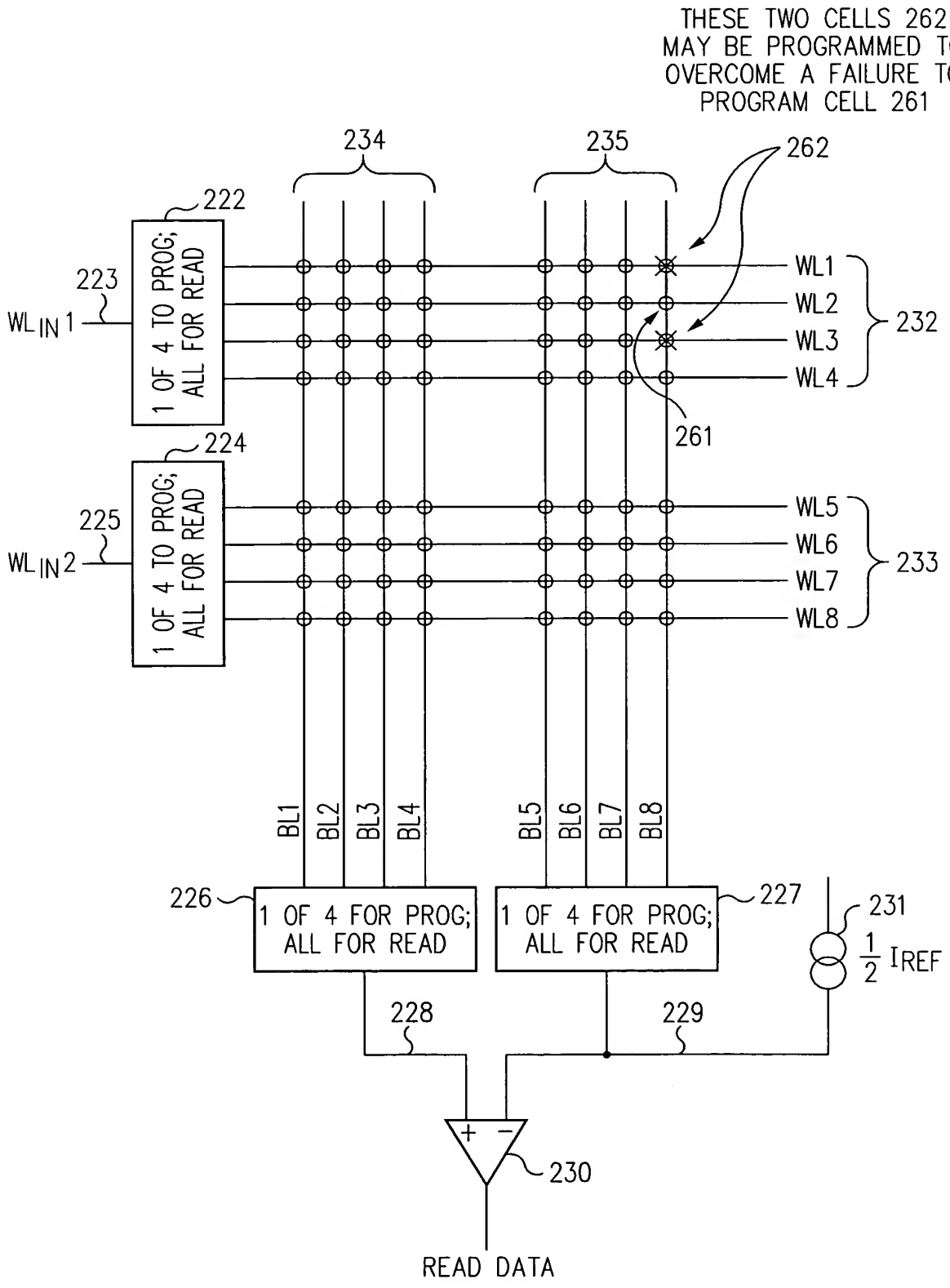

THESE TWO CELLS 262
MAY BE PROGRAMMED TO
OVERCOME A FAILURE TO
PROGRAM CELL 261
234
235
262
222
223
WL IN 1
1 OF 4 TO PROG;
ALL FOR READ
WL1
WL2
WL3
WL4
232
261
224
225
WL IN 2
1 OF 4 TO PROG;
ALL FOR READ
WL5
WL6
WL7
WL8
233
BL1
BL2
BL3
BL4
BL5
BL6
BL7
BL8
226
1 OF 4 FOR PROG;
ALL FOR READ
227
1 OF 4 FOR PROG;
ALL FOR READ
231
1/2 IREF
228
229
+
−
230
READ DATA

FIG. 8

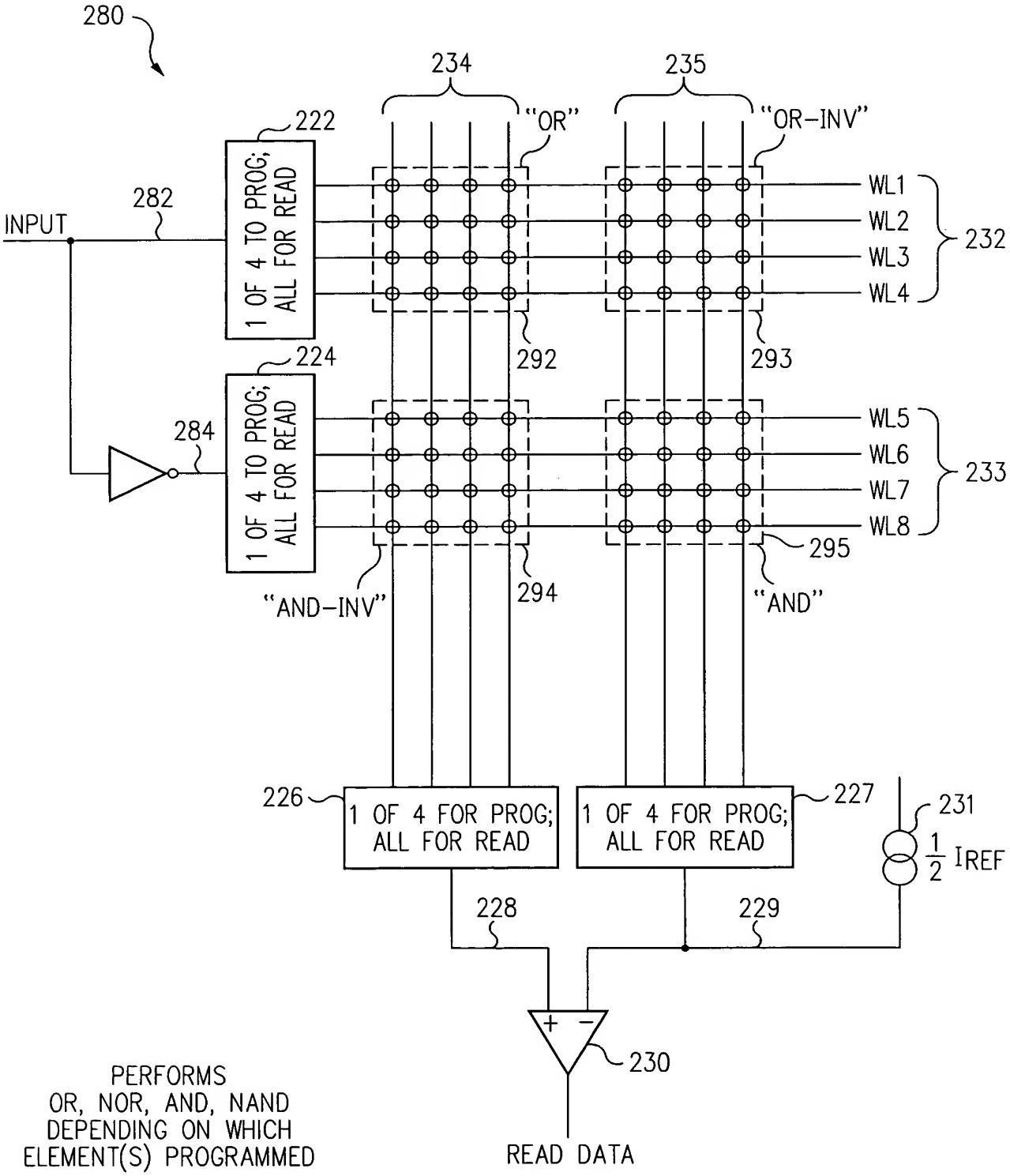

280
234
235
"OR"
"OR-INV"
222
1 OF 4 TO PROG; ALL FOR READ
282
INPUT
WL1
WL2
WL3
WL4
232
292
293
224
1 OF 4 TO PROG; ALL FOR READ
284
WL5
WL6
WL7
WL8
233
295
294
"AND-INV"
"AND"
226
1 OF 4 FOR PROG; ALL FOR READ
227
1 OF 4 FOR PROG; ALL FOR READ
231
1/2 IREF
228
229
230
PERFORMS OR, NOR, AND, NAND DEPENDING ON WHICH ELEMENT(S) PROGRAMMED
READ DATA

FIG. 9

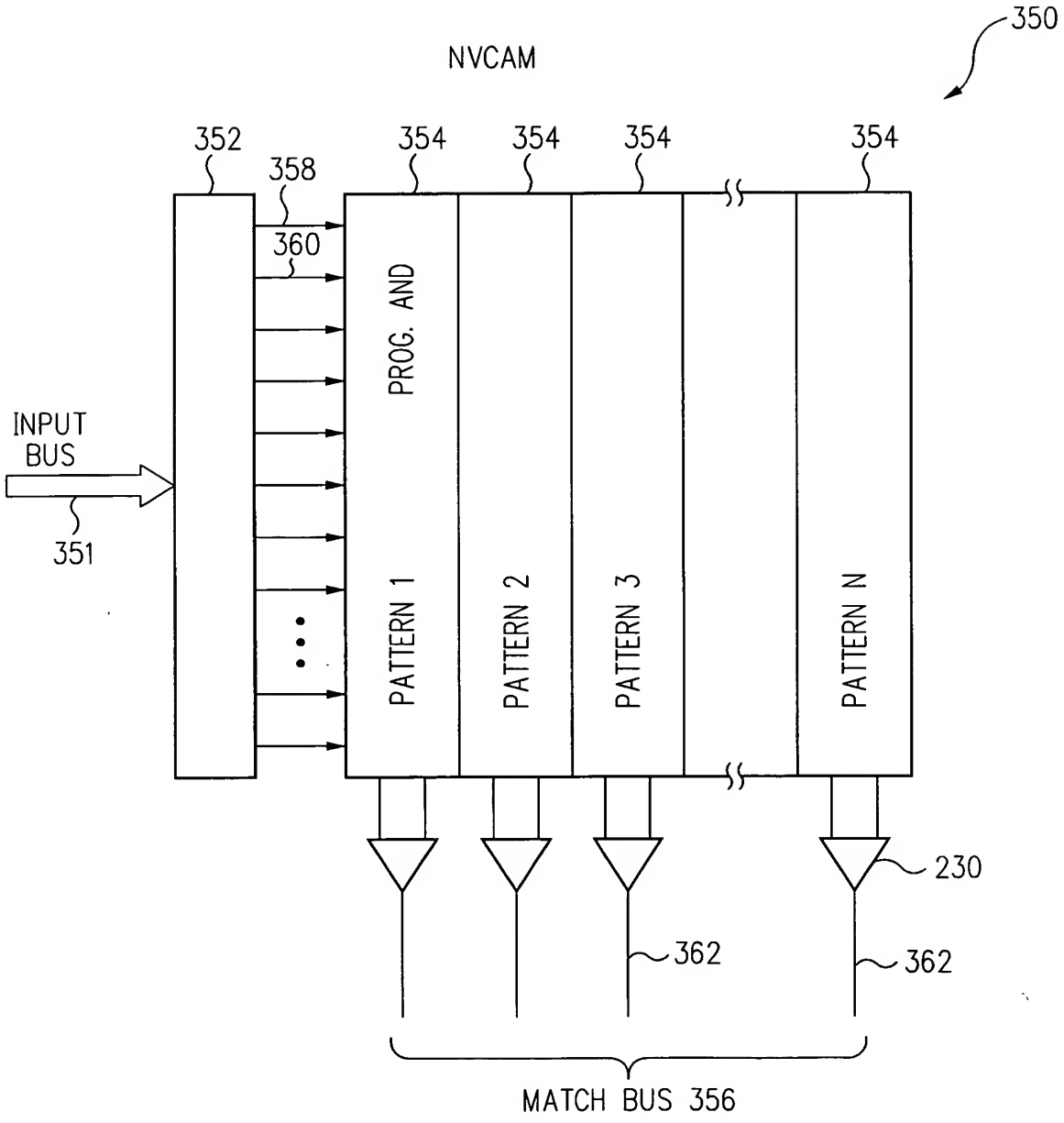

350
NVCAM
352
358
354
354
354
354
360
PROG. AND
INPUT
BUS
351
PATTERN 1
PATTERN 2
PATTERN 3
PATTERN N
230
362
362
MATCH BUS 356

FIG. 10

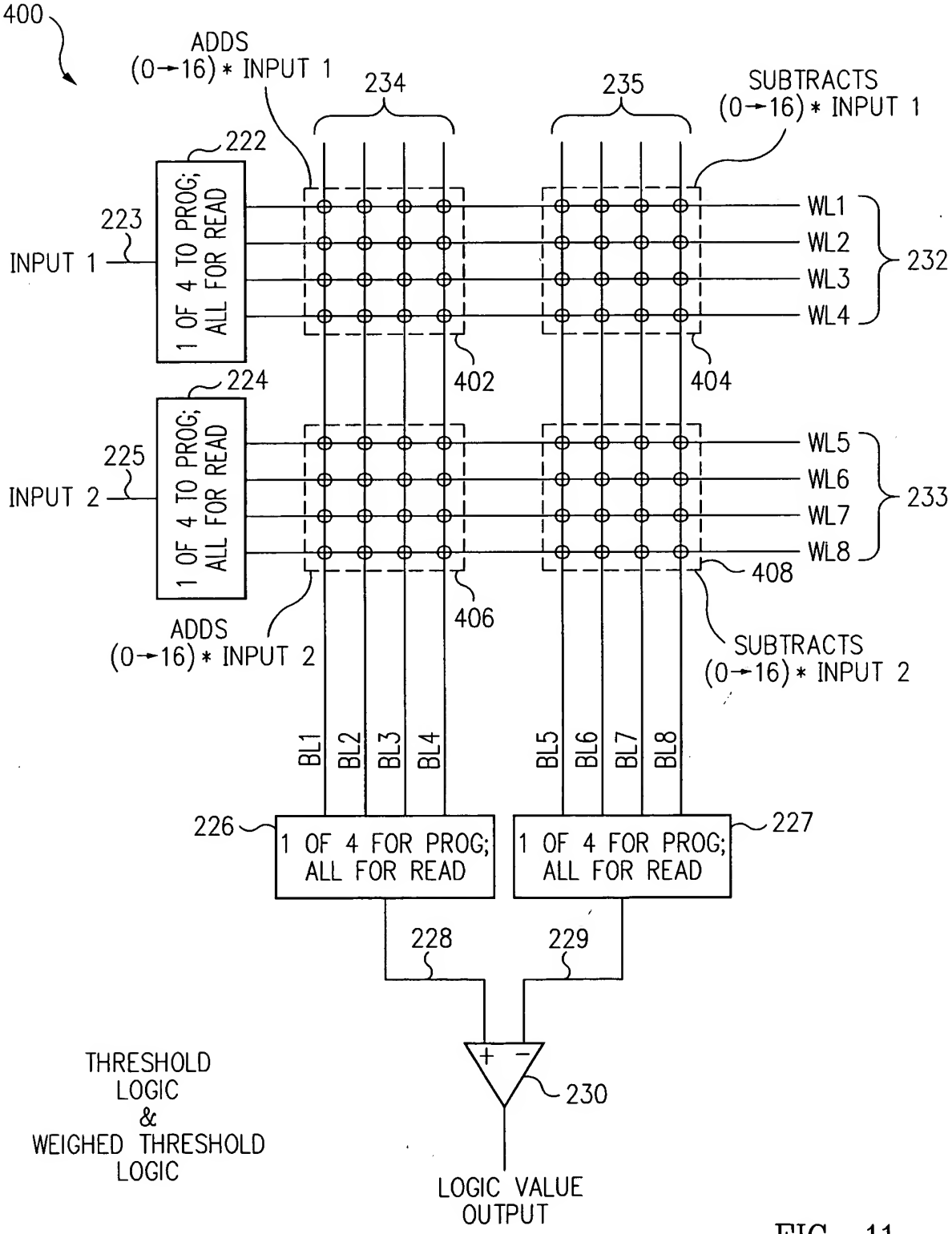

400
ADDS
(0→16) * INPUT 1
234
235
SUBTRACTS
(0→16) * INPUT 1
222
223
INPUT 1
1 OF 4 TO PROG;
ALL FOR READ
WL1
WL2
WL3
WL4
232
402
404
224
225
INPUT 2
1 OF 4 TO PROG;
ALL FOR READ
WL5
WL6
WL7
WL8
233
408
406
ADDS
(0→16) * INPUT 2
SUBTRACTS
(0→16) * INPUT 2
BL1
BL2
BL3
BL4
BL5
BL6
BL7
BL8
226
1 OF 4 FOR PROG;
ALL FOR READ
227
1 OF 4 FOR PROG;
ALL FOR READ
228
229
+
−
230
THRESHOLD
LOGIC
&
WEIGHED THRESHOLD
LOGIC
LOGIC VALUE
OUTPUT

FIG. 11